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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/737,126	12/15/2003	Ken A. Nishimura	10030571-1	5946

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EXAMINER	
THOMAS, BRANDI N	

ART UNIT	PAPER NUMBER
2873	

DATE MAILED: 08/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/737,126	NISHIMURA ET AL.	
	Examiner	Art Unit	
	Brandi N. Thomas	2873	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12,13,15-18 and 20-22* is/are rejected.

7)☒ Claim(s) *11,14 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Detailed Action*.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-10, 12, 13, 15-18, and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gale et al. (5285407) in view of (JP 07-177041).

Regarding claim 1, Gale et al. discloses, in figures 2A, 2B, and 3, a spatial light modulator, comprising: memory elements (32) configured to store data (13, latch circuit) therein and shift data (12, shift register) therebetween (col. 4, lines 7-11, 17-24, and col. 5, lines 5-11) and light modulation elements (21) (col. 5, lines 9-12) but does not specifically disclose the light modulation elements respectively in communication with the memory elements, wherein each of the light modulation elements is alterable in response to the data stored in respective ones of the memory elements. JP 07-177041 discloses, in figure 1, wherein the light modulation elements (22) respectively in communication with the memory elements (43 and 44), wherein each of the light modulation elements (22) is alterable in response to the data stored in respective ones of the memory elements (43 and 44) (sections 0019 and 0021). Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the device of Gale with the modulation elements of JP 07-177041 for the purpose of displaying the stored and shifted data (sections 0019 and 0021).

Regarding claim 2, Gale et al. discloses, in figures 2A, 2B, and 3, a spatial light modulator, wherein said memory elements (32) are arranged in an array having rows and columns (col. 5, lines 5-15).

Regarding claim 3, Gale et al. discloses, in figures 2A, 2B, and 3, a spatial light modulator, wherein said memory elements (32) are configured to shift the data bi-directionally between rows (col. 5, lines 56-61).

Regarding claim 4, Gale et al. discloses, in figures 2A, 2B, and 3, a spatial light modulator, wherein said memory elements (32) are configured to shift the data bi-directionally between columns (col. 5, lines 56-61).

Regarding claim 5, Gale et al. discloses, in figures 2A, 2B, and 3, a spatial light modulator, wherein said memory elements (32) are configured to shift the data bi-directionally between at least one of non-adjacent rows and non-adjacent columns (col. 5, lines 56-61).

Regarding claim 6, Gale et al. discloses, in figures 2A, 2B, and 3, a spatial light modulator, wherein said memory elements (32) are arranged in a nonorthogonal pattern (figure 3).

Regarding claim 7, Gale et al. discloses, in figures 2A, 2B, and 3, a spatial light modulator, wherein said memory elements (32) are static memory elements (col. 6, lines 29-31).

Regarding claim 8, Gale et al. discloses, in figures 2A, 2B, and 3, a spatial light modulator, wherein each of the memory elements (32) includes a feedback element (37) (col. 4, lines 17-25).

Regarding claim 9, Gale et al. discloses, in figures 2A, 2B, and 3, a spatial light modulator, wherein each of the memory elements (32) is a weak feedback element (37) (col. 4, lines 17-25).

Regarding claim 10, Gale et al. discloses, in figures 2A, 3, and 4, a spatial light modulator, further comprising access control elements (34) connected to said memory elements (32) (col. 6, lines 5-15).

Regarding claim 12, Gale et al. discloses, in figures 2A, 3, and 4, a spatial light modulator, wherein each of said memory elements (32) further includes an output node electrically coupled to an electrode (24A and 24B) of said respective light modulation element (21) and to an input node of an additional one of said memory elements (32) (col. 5, lines 33-43).

Regarding claim 13, Gale et al. discloses, in figures 2A, 3, and 4, a spatial light modulator, wherein said memory elements (32) are interconnected in a shift register (12) (col. 4, lines 9-24).

Regarding claim 15, Gale et al. discloses, in figures 1, 2A, and 3, a spatial light modulator, further comprising: a timing circuit (CLK) in communication with each of said memory elements (32) to shift the data between said memory elements (col. 4, lines 13-16).

Regarding claim 16, Gale et al. discloses, in figures 2A, 3, and 4, a spatial light modulator, wherein said timing circuit (CLK) comprises a ripple clock (col. 4, lines 13-16).

Regarding claim 17, Gale et al. discloses, in figures 2A, 3, and 4, a spatial light modulator, it is inherent that a liquid crystal material would be including for the reason being that liquid crystal is used in liquid crystal displays.

Regarding claim 18, Gale et al. discloses, in figures 2A, 3, and 4, a spatial light modulator, wherein said light modulation elements (21) further comprise: a common electrode (24A) configured to receive a common electrodes signal (Node A) for said light modulation elements (21) (col. 6, lines 39-47); and a respective pixel electrode (24B) configured to receive the data stored in said respective memory elements (32) (col. 6, lines 39-47).

Regarding claim 20, Gale et al. discloses, in figures 2A, 3, and 4, a spatial light modulator, wherein said light modulation elements (21) comprise micromirrors (col. 5, lines 46-50).

Regarding claim 21, Gale et al. discloses, in figures 2A, 3, and 4, a spatial light modulator, wherein said memory elements (32) are arranged in blocks, a first one of said blocks configured to receive data from an external input and the others of said blocks configured to receive data from other ones of said memory elements (32) (col. 5, lines 34-43).

Regarding claims 22 and 25, Gale et al. discloses, in figures 2A, 2B, and 3, a method for performing photolithography, said method comprising: altering ones of the light modulation elements (21) in response to the data loaded thereunto to transfer the image onto a substrate (col. 5, lines 9-12); shifting the data between memory elements (col. 4, lines 7-11, 17-24); altering ones of the light modulation elements (21) in response to the data shifted thereunto to transfer the image onto the substrate (col. 4, lines 7-11,

17-24) but does not specifically disclose loading data representing an image into memory elements in communication with respective light modulation elements. JP 07-177041 discloses, in figure 1, loading data representing an image into memory elements (43 and 44) in communication with respective light modulation elements (22) (sections 0019 and 0021). Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the device of Gale with the modulation elements of JP 07-177041 for the purpose of displaying the stored and shifted data (sections 0019 and 0021).

Regarding claim 23, Gale et al. discloses, in figures 2A, 2B, and 3, a method for performing photolithography, wherein each said altering further comprises: applying a voltage in response to the data to the change optical characteristics of the light modulation elements (21) (col. 4, lines 44-61).

Regarding claim 24, Gale et al. discloses, in figures 2A, 2B, and 3, a method for performing photolithography, wherein said shifting further comprises: utilizing a ripple clock to control the timing of said shifting (col. 4, lines 13-16).

Regarding claim 26, Gale et al. discloses, in figures 2A, 2B, and 3, a method for performing photolithography, wherein said altering in response to the shifted data is performed after said moving (col. 5, lines 9-12).

Allowable Subject Matter

3. Claims 11, 14, and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. The prior art taken either singularly or in combination fails to anticipate or fairly suggest the limitations of the independent claim(s), in such a manner that a rejection under 35 U.S.C. 102 or 103 would be proper. The prior art fails to teach a combination of all the claimed features as presented in claim(s) 11, 14, and 19, wherein the claimed invention comprises in claim 11, access control elements including a forward access control element and a reverse access control element; in claim 14, memory elements each include a master-slave flip-flop; in claim 19, a timing circuit that shifts inverted data from a first to a second memory element and switches the common electrode signal, as claimed.

Response to Arguments

5. Applicant's arguments with respect to claims 1-22 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the

advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brandi N. Thomas whose telephone number is 571-272-2341. The examiner can normally be reached on 7- 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Mack can be reached on 571-272-2333. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BNT

BNT

Alicia M Harrington
Primary Examiner
Art Unit 2873